PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L	A2	(11) International Publication Number: WO 99/36941
		(43) International Publication Date: 22 July 1999 (22.07.99)

(21) International Application Number: PCT/US99/00784

(22) International Filing Date: 14 January 1999 (14.01.99)

(30) Priority Data:
60/071,390 15 January 1998 (15.01.98) US

(71) Applicant: CORNELL RESEARCH FOUNDATION, INC. [US/US]; 20 Thornwood Drive, Ithaca, NY 14850 (US).

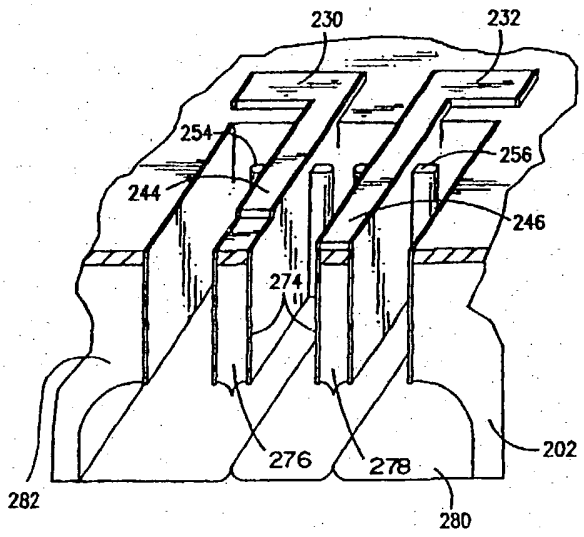
(72) Inventors: ADAMS, Scott, G.; 413 Mitchell Street, Ithaca, NY 14850 (US). SHAW, Kevin, A.; 104 Worth Street, Ithaca, NY 14850 (US). WEBB, Russell, Y.; Apartment 5, 412 S. Albany Street, Ithaca, NY 14850 (US). REED, Bryan, W.; 106 Cayuga Park Road, Ithaca, NY 14850 (US). MACDONALD, Noel, C.; 515 Highland Road, Ithaca, NY 14850 (US). DAVIS, Timothy, J.; 2283 State Route 96, Trumansburg, NY 14886 (US).

(74) Agents: COOPER, George, M. et al.; Jones, Tullar & Cooper, P.C., P.O. Box 2266 Eads Station, Arlington, VA 22202 (US).

(81) Designated States: JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: TRENCH ISOLATION FOR MICROMECHANICAL DEVICES



(57) Abstract

An isolation process which enhances the performance of silicon micromechanical devices incorporates dielectric isolation segments within the silicon microstructure, which is otherwise composed of an interconnected grid of cantilevered beams. A metal layer on top of the beams provides interconnects and also allows contact to the silicon beams, electrically activating the device for motion or transduction. Multiple conduction paths are incorporated through a metal patterning step prior to structure definition. The invention improves manufacturability of previous processes by performing all lithographic patterning steps on flat topographies, and removing complicated metal sputtering steps required of most high aspect ratio processes. With little modification, the invention can be implemented with integrated circuit fabrication sequences for fully integrated devices.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece			TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	NZ	New Zealand		
CM	Cameroon			PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

Trench Isolation for Micromechanical Devices

This invention was made with government support under contract number F30602-97-2-0104 awarded by DARPA. The government holds certain rights in the invention.

This application claims the benefit of U.S. Provisional application No. 60/071,390 filed January 15, 1998, the disclosure of which is incorporated herein by reference.

Background of the Invention

The field of the present invention relates generally to microdevices and microstructures, and more particularly to microfabrication processes to create micromechanical or microelectromechanical devices with integral electrical isolation structures within the devices.

Microelectromechanical systems (MEMS) refers to a technology in which electrical and mechanical devices are fabricated at substantially microscopic dimensions utilizing techniques well known in the manufacture of integrated circuits. Present commercial applications of MEMS technology are predominantly in pressure and inertial sensing, with an emphasis on automotive applications thereof. For an introduction to the use of MEMS technology for sensors and actuators, see for example the article by Bryzek et al. in *IEEE Spectrum*, May 1994, pp. 20-31.

The fabrication processes for MEMS, called micromachining, are borrowed from the integrated circuit industry, where semiconductor devices are fabricated using a sequence of patterning, deposition, and etch steps. Surface micromachining

has typically used a deposited layer of polysilicon as the structural micromechanical material. The polysilicon is deposited over a sacrificial layer onto a substrate, typically silicon, and when the sacrificial layer is removed the polysilicon remains free standing. Bulk micromachining techniques, rather than using deposited layers on a silicon substrate, etch directly into the silicon wafer to make mechanical structures of the single crystal silicon itself. Bulk micromachining was first practiced using anisotropic wet chemical etchants such as potassium hydroxide, which etch faster in certain crystallographic planes of silicon. However, advancements in reactive ion etching (RIE) technology have made practical, and in many ways preferential, the use of dry plasma etching to define micromechanical structures. Reactive ion etching techniques are independent of crystal orientation, and can create devices exceeding the functionality of surface micromachined devices. The use of single-crystal materials, particularly silicon, can be beneficial for mechanical applications because of the lack of defects and grain boundaries, maintaining excellent structural properties even as the size of the device shrinks.

Deep reactive ion etching techniques developed specifically for the MEMS industry have enabled a greater range of functionality for bulk micromachining. Processes such as those described in US Patent No. 5,501,893 are now supplied by commercial etch vendors specifically for bulk micromachining. These processes provide silicon etch rates in excess of 2um/min with vertical profiles and selectivity to photoresist greater than 50:1 or selectivity to silicon oxide greater than 100:1. This enables bulk micromachined structures to span the range from several microns deep to essentially the thickness of an entire wafer (>300um).

The predominant difficulty in bulk micromachining is the requirement for most devices that the silicon of the microstructure be mechanically connected to but electrically isolated from the substrate silicon. In particular, if the device is electrically

activated or transduced, the current path from the structure to the substrate must be reduced or effectively eliminated in order that the device function appropriately. This requirement has proven to be the most difficult to achieve in fabrication.

An example of a process for bulk micromachined structures is described in U.S. Patent No. 5,719,073 which is assigned to the assignee of the present application, the disclosure of which is hereby incorporated herein by reference. This process uses a single mask layer and appropriate etch and deposition steps to create a fully self-aligned, metalized bulk micromachined structure. Reactive ion etching is used to define and undercut an array of cantilever beams, which are connected together in order to form a more complete functional microstructure. All structure elements and interconnects are formed with the same masking layer, and isotropic dry etch techniques are used to release the structural layer. The advantages of the process are the simplicity of the single masking layer, the reactive ion etch release process, the self-aligned metalization, and high manufacturing yield.

The process flow for the '073 patent defines a pattern in a dielectric mask which is transferred to the single crystal material substrate by a 10-20um trench etch. After the sidewalls of the trench are protected using a second dielectric layer, such as silicon dioxide, the silicon islands or mesas are undercut and released using an isotropic reactive ion etch. The released silicon mesas essentially become the cantilever beams. A final self-aligned metal layer is deposited onto the oxide layer on the beams, allowing electrical connection to the structure. The process of the '073 patent can be carried out on a wafer having existing integrated circuitry, in which case the individual process steps are all performed at a temperature of less than 300°C.

With the self-aligned metal layer of the '073 patent, only one electrical connection is made to the microstructure. In situations where several connections are necessary, additional photolithography or masking steps must be performed on the released structure. These additional steps limit device yield, since photoresist application on and removal from a released microstructure often results in device failure. Although the metal layer of the '073 patent is self-aligned, it has been found that evaporation or sputtering of metal on the sidewalls of 10-20um deep beams is a difficult, non-standard process step, and the resulting metal layer is often highly nonuniform in thickness and will coat only a portion of the total beam depth. Further, a metal-oxide-silicon interface is a source of parasitic capacitance for those devices which rely on opposing metal layers for capacitive actuation and transduction and the large area provided by the beam sidewalls in the '073 patent and the metal-oxide-silicon beam structure directly results in a large parasitic capacitance. For many inertial sensing devices, the variable capacitance provided by opposing beam sidewalls is actually exceeded by the parasitic capacitance to the substrate silicon.

An attempt to modify the process of the '073 patent to reduce the level of parasitic capacitance, and thus improve the device performance resulted in the invention described in U.S. Patent No. 5,426,070, also assigned to the assignee of the present invention. Here, an oxidation step is carried out to consume sections of the silicon beams, converting these sections completely to oxidized segments. As a result, the remaining silicon of the microstructure is electrically isolated from the substrate silicon by an oxide beam segment. However, the thick oxide layer required for the insulating segment is also grown on sidewall surfaces of the surviving silicon beams, drastically modifying the mechanical performance of the composite beams. In addition, the self-aligned metalization creates only one contact to the microstructure and since the metal is required to coat the sidewalls of the beams,

the result is the non-uniform and unreliable metal coverage described above.

Other techniques for providing isolation and parasitic capacitance reduction for bulk micromachined devices have been attempted. Many have relied on the use of specially prepared substrates such as silicon-on-insulator, where the wafer has a built-in buried oxide layer. The microstructure is formed from the silicon layer existing on the top of the buried layer, and released using chemical etching of the buried layer. However, the chemical etch to release the silicon microstructure has relatively low yield, and the substrate itself is specialized and expensive. In Brosnihan, et al., "Embedded interconnect and electrical isolation for high-aspect-ratio, SOI inertial instruments," *Transducers 97*, pp. 637-640, the authors combine the SOI substrate with nitride and polysilicon isolation blocks. However, the structure definition and release still depend on the buried SOI layer and the resulting expensive substrate preparation.

As bulk micromachined devices increase in complexity it becomes increasingly important to improve their electrical performance. Multiple electrical connections are required for more complex MEMS devices. Electrical isolation between the various connections, and between the structure and the substrate, are also required. Typically such isolation is accomplished in the prior art by separating conducting metal layers by insulating dielectric layers. See for example U.S. Patent No. 5,611,940. It is also well known in the prior art to provide dielectric isolation regions between microelectronic devices or conductors in integrated circuits, as in U.S. Patent Nos. 4,688,069 and 4,876,217. A particularly beneficial approach to electrical isolation has been the use of trenches filled with insulating material, described in U.S. Patent Nos. 4,104,086, 4,509,249, 4,571,819, and 4,519,128. Although the electrical isolation schemes in the prior art are very satisfactory for conventional integrated circuit devices, they have serious shortcomings when

applied to microelectromechanical devices.

MEMS devices contain moving mechanical microstructures, typically exhibiting substantially three-dimensional geometries. The existence of these structures precludes, or makes very difficult, the application of electrical isolation schemes such as those described in the prior art. Such schemes involve multiple steps of lithography, etching, and deposition. These steps are not feasible on structures exhibiting large topographic variations, nor on microstructures which have been previously released for motion.

What is required for effective electrical isolation in MEMS devices is a new electrical isolation process which must be compatible with the specific requirements and limitation of MEMS devices, most notably the existence of released, movable microstructures.

What is also required of the electrical isolation process is that it provide isolation between adjacent mechanical structures, between different electrical segments, and between the device and the substrate material. In bulk micromachining, this most often means breaking the electrical continuity between the structure silicon and the substrate silicon. It is desired that such an isolation structure should also provide for reduced parasitic capacitance in the device. MEMS sensors typically require the ability the measure very small changes in electrical charge or capacitance, and therefore must minimize the effect of parasitic circuit elements.

Further what is needed is an electrical isolation process which does not have an adverse impact on the manufacturing yield of MEMS devices. The commercial viability of MEMS technology depends on cost effective manufacturing of products. Prior art electrical isolation schemes may result in very low manufacturing yields and

hence unacceptably high costs for most MEMS product applications.

Summary of the Invention

In order to achieve the foregoing and to overcome the problems inherent in prior electrical isolation schemes, the present invention is directed to a beam-level isolation technique in which insulating segments are incorporated within silicon beam microstructures to provide electrical isolation.

It is therefore an object of the present invention to provide suitably modified trench isolation techniques, utilizing dielectric materials, in conjunction with micromechanical device fabrication processes to achieve electrical isolation within the microstructure.

It is a further object of the invention to eliminate the use of unsuitable and unreliable sidewall metal layers for electrical activation of a MEMS device, and instead to use the silicon cores of microstructure beams for conduction and as capacitor plates. This is achieved by creating contacts from a metal layer through a dielectric layer to the silicon beams using techniques which are common in the art.

It is a further object of the invention to provide multiple metal interconnections within a MEMS device. This is achieved by placing metal conductor lines over isolation segments and on top of cantilever beams to provide multiple metal paths. The conductor lines are separated from the core silicon by an insulating layer which is also present on top of the beams, thus achieving isolation between the metal and the silicon.

It is a further object of the invention to alleviate dielectric-induced stress on silicon beam microstructures by minimizing the amount of sidewall film present on

the silicon. Thermal oxidation of existing beam structures creates a thick sidewall oxide film which dominates device characteristics. By performing isolation processes before structure formation, sidewall films can be reduced or even eliminated, and hence passivation films can be rendered unimportant to device performance.

It is a further object of the invention to provide a trench isolation process for fabricating microstructures which is scalable to different structure etch depths, while maintaining high manufacturing yield. The trench isolation process may be scaled to etch depths greater than 50um using deep reactive ion etching techniques, and can be adjusted to a particular microstructure depth. Planar lithography for the isolation segments, metal deposition, and structure definition maintains high manufacturing yield and does not deviate from techniques common to the semiconductor processing industry.

Although the preferred embodiment of the invention is to use thermal oxidation to form the isolation segments, other lower temperature chemical vapor deposition techniques can also be used for trench isolation. Further, even with high temperature oxidation steps, it is possible to integrate the micromechanical isolation process with integrated circuits without significant interleaving of the process steps.

Briefly, the basic process begins by defining an isolation trench pattern for a desired micromechanical structure on an oxide coated silicon wafer. The pattern defines the region, or regions, where dielectric isolation segments will be placed. These dielectric segments serve to separate the silicon of the micromechanical structure from the silicon of the substrate. The pattern for the dielectric segments present in the exposed photoresist is transferred to the oxide underlayer using a reactive ion etch. Then, an isolation trench is defined in the wafer using silicon

reactive ion etching, typically 1-1.5um wide and 10-50um deep into the substrate silicon. The shape of the trench, or the trench profile, is optimized to improve the isolation properties of the segment in conjunction with the remainder of the microstructure processing steps. In the preferred embodiment, the trench profile is reentrant, with a wider width at the bottom of the trench than at the top of the trench. The purpose of shaping the trench is to reduce the possibility of silicon filaments forming during the remainder of the processing. Such filaments may surround the isolation segment and provide a leakage path which reduces the efficacy of the isolation.

After the isolation trench is defined, the trench is filled with a dielectric, preferably with a thermal oxidation step. Alternatively, the trench may be filled using chemical vapor deposition techniques with silicon dioxide or silicon nitride. During thermal oxidation, the silicon sidewalls of the trench are consumed to form silicon dioxide, and the resulting volumetric expansion narrows the trench opening to effectively fill the trench. Because of the high aspect ratio of the trench, a void is often formed within the dielectric. Unlike most electrical isolation schemes, however, the void is unimportant to device operation.

After the trench is filled, the wafer surface has small topography variations around the locations of the isolation segments. Therefore, a planarization step is performed, normally with photoresist, to smooth the surface of the wafer and prepare it for the patterning and deposition steps to follow. An application of resist or other viscous material, and subsequent etchback, is used to planarize the small nonuniformities in the surface and reduce the thickness of the dielectric on the surface of the wafer.

Next, a second masking layer defines vias in locations where connection is to

be made from a subsequent metal layer to the silicon beam structures or the silicon substrate. Eventually, metal to silicon contacts are made through the vias as is typical of integrated circuit processing. The via pattern in the photoresist is transferred to the silicon oxide using RIE processes, and the silicon surface is exposed for contact processing. After implantation and annealing of dopants, the metal layer is sputter deposited. The metal layer forms the contacts to the underlying silicon and is also used, in conjunction with further processing, to create multiple interconnections to the micromechanical device.

A third photolithography step coarsely patterns the metal in preparation for the final structure etches. The coarse metal pattern is transferred to the metal layer using a wet chemical etch step or a dry reactive ion etch. The coarse metal patterning step removes metal from the regions where the interconnections are to be broken. A final lithographic patterning step defines the micromechanical structure in the form of an interconnected grid of silicon beams. The beams are created by transferring the photoresist pattern through the metal and dielectric masking layers. Silicon islands or mesas are defined using a silicon trench etch which surrounds the mesa features. After the sidewalls of the beams are passivated using a dielectric layer, the beam features are released using an isotropic reactive ion etch. The sidewall passivation layers can be removed, if desired, by another isotropic reactive ion etch, etching dielectric preferentially to silicon.

In summary, the process of this invention creates a silicon structure similar to those developed in the '703 patent, but offering several substantial advantages. A metal conductive layer is present on the top of the beam structures only. Isolation segments are incorporated into the silicon beams, reducing parasitic capacitance and providing multiple structure connections. In regions where capacitive actuation or sensing is required, the metal layer contacts the beam silicon cores, which serve

as the capacitor plates. This is allowed because the isolation segments interrupt the conduction path from the silicon beams to the substrate silicon. Multiple conduction paths are possible using the top conductive metal layers and the contacts to the underlying silicon. The process is greatly improved from the prior art because a sidewall metal layer is not required, and multiple connections to the released microstructure are possible. The process is inherently manufacturable because all photolithography steps are performed on a flat surface, and none are performed on a released structure. The process can be merged with integrated circuits to create fully integrated systems on a chip.

Brief Description of the Drawings

The foregoing and additional objects, features, and advantages of the present invention will become apparent to those of skill in the art from the following detailed description of a preferred embodiment thereof, taken with the following drawings, in which:

Figures 1a-1h diagrammatically illustrate the basic trench isolation process of the invention:

Figures 2a-2i illustrate the basic process in perspective view;

Figure 3 is a photomicrograph showing the isolation segments and metal conduction layer on a released microstructure;

Figure 4 illustrates a multiple level interconnect scheme resulting from the basic process;

Figures 5a-5h illustrate a method to implement the isolated microstructure with an integrated circuit; and

Figures 6a-6i illustrate an alternative method to merge the microstructure process with an integrated circuit.

Detailed Description of the Invention

Although a number of variations of the invention are possible, the basic process is illustrated in Figures 1A-1H, which show in cross section the steps for fabricating from a silicon wafer a single released micromechanical beam with a single incorporated isolation segment. It will be understood from the process outlined in subsequent sections, that an entire micromechanical structure may be composed of any number of such beams, connected to each other and/or to the wafer in a manner to provide full device functionality.

Referring to Figure 1A, a silicon wafer 102 is provided with a dielectric layer 104, preferably silicon dioxide (oxide). The silicon wafer can be of arbitrary doping, resistivity, and crystal orientation, since the process depends only on reactive ion etching to carve and form the structures. The layer 104 serves the function of protecting the silicon surface of the wafer during an isolation trench etch to follow, and thus represents a masking layer only. This masking layer can be formed from any number of techniques, including thermal oxidation of silicon or chemical vapor deposition (CVD). The typical thickness of the masking layer 104 is 0.5-1.0um. A photoresist 106 is then spun onto the wafer and exposed and developed using standard photolithography techniques to define the isolation trench pattern 108. Reactive ion etching is used to transfer the photoresist pattern to the mask layer 104,as at 110, exposing the silicon surface 112. Typically, the silicon dioxide mask is

etched in a Freon gas mixture, for example CHF_3 or CF_4. High etch rates for silicon dioxide etching are achieved using a high density plasma reactor, such as an inductively coupled plasma (ICP) chamber. These ICP chambers use a high power rf source to sustain the high density plasma and a lower power rf bias on the wafer to achieve high etch rates at low ion energies. Oxide etch rates of 200nm/min and selectivities to photoresist greater than 1:1 are common for this hardware configuration.

As illustrated in Figure 1B, an isolation trench 114 is next formed in the wafer 102 by deep reactive ion etching of silicon using high etch rate, high selectivity etching. The trench is commonly etched in a high density plasma using an SF6 gas mixture as described in patent 5,501,893. Preferably, the etch is controlled so that the trench profile is reentrant, or tapered, with the top 116 of the trench being narrower than the bottom 118 of the trench. This tapering ensures that good electrical isolation is achieved in subsequent processing. Profile tapering can be achieved in reactive ion etching by tuning the degree of passivation, or by varying the parameters (power, gas flows, pressure) of the discharge during the course of the etch. Since the trench is to be filled with dielectric, the opening at the top 116 of the trench is chosen to be less than 2um in width. The trench depth is typically in the range 10-50um. A common procedure for etching the trench is to alternate etch steps (SF_6 and argon mixture) with passivation steps (Freon with argon) in an ICP plasma to achieve etch rates in excess of 2um/min at high selectivity to photoresist (>50:1) and oxide (>100:1). The power and time of the etch cycles are increased as the trench deepens to achieve the tapered profile. Although the trench geometry is preferably reentrant, arbitrary trench profiles can be accommodated with adjustments in microstructure processing. Good isolation results can be achieved with any of a number of known trench etch chemistries. After the silicon trench is

etched, the photoresist layer 106 is removed with wet chemistry or dry ashing techniques, and the masking layer 104 is removed with RIE or buffered hydrofluoric acid.

Referring to Figure 1C, the isolation trench 114 is then filled with an insulating dielectric material, typically silicon dioxide. The filling procedure results in the mostly solid isolation segment 120 in the trench 114, and serves to deposit a layer 122 of dielectric material on the top surface 112 of the silicon wafer and dielectric layers on the sidewall 124 and bottom 126 of the trench. The thickness of the deposited layer is usually in excess of 1um. This fill can be accomplished with chemical vapor deposition (CVD) techniques or preferably with oxidation of silicon at high temperatures. In thermal oxidation, the wafer is exposed to an oxygen rich environment at temperatures from 900-1150°C. This oxidation process consumes silicon surfaces to form silicon dioxide. The resulting volumetric expansion from this process causes the sidewalls of the trenches to encroach upon each other, eventually closing the trench opening. In a CVD fill, some dielectric is deposited on the walls but filling also occurs from deposition on the bottom of the trench. CVD dielectric fill of trenches has been demonstrated with TEOS or silane mixtures in plasma enhanced CVD chambers and low pressure CVD furnace tubes.

During a trench fill, it is common for most trench profiles to be incompletely filled, causing an interface 128 and a void 130 to be formed in the trench. A local concentration of stress in the void can cause electrical and mechanical malfunction for some devices, but is generally unimportant for micromechanical devices due to the enclosed geometry of the isolation segment 120. The interface 128 and void 130 can be eliminated by shaping the trench to be wider at the trench opening 116 than the trench bottom. However, good electrical isolation would then require additional tapering of the microstructure trench etch in later steps. Another artifact of the trench

filling is an indentation 132 that is created in the surface of the dielectric 134, centered over the isolation segment 120. This indentation is unavoidable in most trench filling processes, and can be as deep as 0.5um, depending on the thickness of the deposition.

To remove the indentation 132, the surface is planarized to form a flat surface 136, as illustrated in Figure 1D, for subsequent lithographic and deposition steps. Planarization is performed by depositing a viscous material, which can be photoresist, spin-on glass, or polyimide, and flowing the material to fill the indentation 132 to a smooth finish. During etchback, which is the second step of planarization, the surface 136 is etched uniformly, including the filled indentation. Therefore, by removing part of the surface oxide 122, the indentation 132 is removed to create a uniform thickness layer 138. For example, if the original dielectric layer 122 is 2um, then planarization to remove the indentation 132 leaves a dielectric layer 138 having a final thickness of less than 1um. The surface 136 of the wafer is free from imperfection and is ready for further lithography and deposition.

In Figure 1E, a second photolithography step opens vias to prepare contacts to the underlying silicon 102. This second lithographic step is performed by exposing and developing a pattern of via openings 140 in a layer of resist 142 on surface 136 and transferring the pattern into the underlying dielectric layer 138. After lithography, the silicon is implanted in the region 144 using dopants matched to the substrate silicon 102. A high concentration of dopants, either p or n type, in the region 144 will serve to create an ohmic contact between the silicon and a metal layer on the surface of dielectric layer 138. The silicon region 144 may be protected from implant damage by leaving a thin layer of dielectric at the surface 146 of the silicon. After the silicon is implanted, the resist 142 is removed with wet chemicals or ashing and the

wafer is annealed to activate the implanted ions.

A sputtered metal layer 148, preferably aluminum, is deposited in Figure 1F. The metal covers the surface 136 of the dielectric 138, and uniformly coats over the isolation segment 120 as a result of the planarizing step. The metal layer fills the via 140 and contacts the implanted region of silicon at 144, electrically connecting the metal to the silicon to form an ohmic contact. Otherwise the metal layer is insulated from the substrate silicon 102 by means of the dielectric layer 138. The thickness of the metal layer is nominally 0.5um, although arbitrary thickness is acceptable. Sputtering is preferably used instead of evaporation because of the ease of volume production. As known in the prior art, some silicon or copper content in an aluminum layer, or target, will improve resistance to electromigration-induced failure.

A third photolithography step is shown in Figure 1G. Lithography is performed with a spun on resist layer 150 on the top surface of the metal layer 148. The resist is patterned to provide open areas 152 where metal is not desired; this step is referred to as coarse metal patterning. The opening 152 in the resist is transferred to the metal layer 148 by wet chemical etching or reactive ion etching. For aluminum RIE, a combination of BCL_3 and CL_2 in a parallel plate etcher is known in the art. The etch is stopped at the surface 136 of the oxide layer 138. The removal of metal at the opening 152 separates the region of metal 156 from the region of metal 158 on the top of an individual beam element. This is important in situations where multiple interconnection paths are required to and on the micromechanical structure.

The micromechanical beams are created, as illustrated in Figure 1H, by applying the techniques of the '703 patent. Thus a final, fourth lithographic step is applied using photoresist layer 160, which is patterned to define an array of beam

previously defined on the top surface. The bottom surface 62 is covered by an oxide layer 78 which may be in place as a result of the initial thermal oxidation of the wafer during processing of the front (top) surface. If no oxide layer is present, a layer may be deposited through chemical vapor deposition techniques, and a photolithography process is performed using a thick (greater than 5 micrometers) photoresist layer 80 on the oxide layer 78. The photoresist is exposed using a double-side mask aligner so that the exposure on the bottom surface of the wafer is accurately aligned with the existing patterns on the top surface of the wafer. The photolithography step defines a pattern 82 that will be etched into the bottom surface of the wafer to define the perimeter of the suspended silicon block 10. This pattern is aligned with the top surface pattern so as to cooperate with the top surface trench to produce a through trench which extends through the wafer and surrounds a desired through-wafer structure. When maximum mass is desired, as in an accelerometer application, the resulting block of silicon has the same thickness as the wafer. When a lesser mass is desired for the block, the bottom surface trench can be widened to define an area of the bottom surface over which the wafer will be thinned, as may be desired when the large area block is to be used as a scanning platform, as for data storage or recovery. The photolithography pattern created in the photoresist layer is transferred to the bottom surface oxide layer 78 using a standard oxide etching process.

As illustrated in Fig. 6, a bottom surface etch is then performed through the pattern 82, as by using the Bosch silicon etch technique described above, to carve out a bottom surface trench 84 which extends around the periphery of the region 86 of the wafer which is to become the large area block or platform. As illustrated, the bottom

surface of the region 86 is protected from the etch by the portion 87 of the patterned oxide layer 78 when the full thickness of the region 86 is to be maintained. The etching of trench 84 is stopped short of the floor 76 of the trenches 70 formed in the top-surface etching so as to prevent the region 86 from being freed from the substrate during this step. Normally, this is done by timing the bottom surface etch to insure that the floor 88 of trench 84 stops 10-30 micrometers away from the floor 76. If the substrate 12 is 400 micrometers thick, and if the trenches 70 are etched to a depth of 30 micrometers, the target etch depth for the trench 84 would be approximately 350 micrometers.

The device is completed, as illustrated in Fig. 7, by finishing the top surface processing. First, if a protective layer of photoresist has been spun on to the etched features on the top surface, that photoresist layer is removed using a wet (chemical) or dry (plasma) etched process. Thereafter, a blanket oxide etch is performed in order to remove the passivation oxide layer 74 from the horizontal surfaces of the substrate, thus exposing the silicon at the floor 76 of the trenches 70 and a trench etch is performed in order to extend the depth of the trenches 70. This serves to expose more silicon at the bottom of the trenches and beneath the side wall oxide layer 74, as illustrated at 94, in order to facilitate the later release of the mesas, but also serves to join the portions of top trench 70 which surround the periphery of region 86 and which are aligned with the bottom trench 84 with the bottom trench to produce a through trench, indicated at 96, which extends completely through the wafer. The through trench 96 forms a cavity in the wafer to thereby release the large area region 86, except where it is joined to the substrate by the mesas which will form the flexible

support structures or actuators, as at bridges 97.

Thereafter, as illustrated in Fig. 8, an isotropic silicon release etching step is performed, based on SF_6 in an ICP plasma, in trenches 70. This completes the structure by undercutting the mesas 71 and 72, as illustrated at 100, to create cantilever beams 102 and 104 which are joined together at one end, as illustrated at 105 in Fig. 9, and which are secured at bridges 97 to the substrate 12 and to the now-released large area region 86 which forms the block 10 discussed above. This undercutting step may also serve to remove any remaining thin layer of silicon surrounding the large area region 86. The final released device is thus comprised of a large area silicon mass 86 which may be the thickness of the original wafer 12 and which is attached to and is integral with the wafer and is suspended in a cavity in the wafer by a cantilever beam array 106 formed from the released mesas 71 and 72.

A metal layer 110 may be sputtered onto the exposed surfaces of the substrate, the large area mass 86 and the flexible support arm array 110, as illustrated in Fig. 8, to provide conductive surfaces for use in activating the device or for providing sensors to detect motion. The metal coats the tops and sidewalls of the structure as well as a portion of the exposed floor of the substrate, as illustrated. The undercut portion indicated at 112 breaks the electrical path between the coating on the floor of the substrate and the coating on the top surface and sidewalls.

If a thinner large area mass 86 is desired, the masking step at the bottom surface of the substrate illustrated in Fig. 5 would be modified; for example, by

removing the mask from the region 87, which in the process of Fig. 5 defines the location of the block to be sopported in the cavity. By removing this region of the mask, the etching step of Fig 6 would enlarge the trench 84 to extend completely across the area of the region 86 (or across any desired portion of it, as defined by the mask), and as a result, the surface 88 illustrated in Fig. 6 would form the bottom surface of the block as illustrated by the dotted line 114, and the thickness of the block would be equal to the distance between surface 88 and the top surface 60 of the original substrate as indicated by the distance *d* in Figs. 6 and 7. This thinner block would be suitable as a movable platform for applications where a wide range of motion is desired, as indicated above.

Although the process has been described as including the application of a metal layer 110, it will be understood that if desired a more complicated process can be used where, instead of providing a final layer of metal, a patterned metal interconnect on top of an oxide layer on the silicon beams can be provided. This would allow the beams themselves to be used as capacitor electrodes by electrically isolating them from the substrate by oxide isolation segments transverse to the beams.

The process of Figs. 3-8 results in a high mass solid silicon block cut out of a silicon wafer and suspended in a cavity extending through the full thickness of the wafer. The mass inherent in such a structure is 100-1000 times that of a silicon device fabricated by the SCREAM-1 process described above and used to fabricate high aspect ratio, thin beams such as the flexible connector array 106 illustrated in Fig. 8. Since the large area device can have dimensions in the millimeter scale rather

beams according to the '703 patent by a sidewall passivation scheme. A dielectric, preferably silicon dioxide, is deposited using CVD techniques and forms a thin film on all surfaces. The thickness of the deposited film is less than 500nm, and must be deposited at a temperature which will not harm the metal layer 228. Preferably, the film which will form the sidewall passivation dielectric is deposited using PECVD or HDPCVD techniques and conformally coats all exposed surfaces. After the deposition, a blanket anisotropic RIE etch removes the film from the floor 270 of the trench 258 and from all other horizontal surfaces, such as the top surface 272 of the metal layer 228. Due to the anisotropic nature of the etch, sidewall films 274 of the mesas remain intact to provide sidewall passivation which protects the silicon mesas 260 and 262 from the isotropic silicon release etch processes.

Figure 2I illustrates a released microstructure after a release etch sequence which follows sidewall passivation. Often, the release etch is comprised of two separate etches; a trench extension which exposes a larger silicon surface area and an isotropic release etch which undercuts the silicon mesas to form released beams 276 and 278. The trench extension is similar to the structure etch of Figure 2G, and deepens the trench 258 to expose silicon below the sidewall film 274. This is followed by an isotropic release etch which can be performed in a high density etch chamber in a mixture of SF_6 and Argon. The release etch is timed so that beams 276 and 278 are completely undercut and suspended over the silicon floor 280, while wider features such as wall 282 remain fixed to the substrate. The isolation segments 254 and 256 extend downwardly through the beams, as illustrated in Figure 1H, to isolate the silicon of the beams 276 and 278 from the silicon of the substrate 202. The metal pads 230 and 232 are connected to the beams at selected via locations by means of interconnects 244 and 246, resulting in multiple conduction paths or multiple connections to the microstructure. It is understood that the beams

276 and 278 preferably are a part of a larger micromechanical structure with an array of similar beams and interconnects, and are intended only to represent the isolation process. The sidewall films 274 can remain on the microstructures or be removed by an isotropic dielectric etch. In general, the sidewall passivation film can be removed if its presence affects the behavior of the micromechanical structure.

Figure 3 is a photomicrograph of a portion of a released 20um tall micromechanical structure employing the isolation segments of the invention. The released structure 302 consists of a grid of cantilever beams 304 with crossbeams 306 for support of the array. The isolation segments 308 separate the portions 310 of the silicon beams to the left of the segments from the portions 312 of the beams to the right of the segments. Conductive metal layer 314 runs along the top of each beam, except in the regions 316 where the metal layer has been broken during the coarse metal patterning step. As a result, the conducting path 318 is separate from the conducting path 320. It is understood that this is only a portion of the overall micromechanical structure, and that numerous geometries and conduction paths are possible using the herein disclosed technology.

The process of the basic invention provides a great deal of functionality. As an example, a multiple level electrical interconnect results from the basic process without any additional fabrication steps. Figure 4 illustrates a multiple level interconnect with the intersection of two silicon beams 402 and 404. Beam 404 has integral electrical isolation segments 406 and 408, a dielectric top layer 410, and a metal layer 412. Conduction through the continuous metal layer 412 allows current to flow from one end of the metal line 414 to the other end 416. This current or applied potential is isolated from the silicon beam 404 beneath by means of the insulator 410. Another electrical conduction path is provided by the cross beam 402 through electrodes 418 and 420, by means of the metal-silicon contacts 422 and

424. Current flows from the metal conductor 418 through the contact 422, through the silicon beam portions 426 and 428, back through the contact 424 and out the metal conductor 420. Since the silicon beam segment 430 is fixed to beam segments 426 and 428, it remains part of the conduction path. However, the silicon beam segments 432 and 434 are isolated from the conduction path by means of isolation segments 406 and 408.Therefore, a two level contact path is allowed; one through the metal layer 412 and the other through the silicon beam 402. Whereas other processes require additional masking layers to create two or more levels of interconnection, the electrical isolation process described above contains all the processing required to form a multiple level interconnect using the silicon beam microstructures.

It is often advantageous to merge micromechanical structures with integrated circuits for control of actuation or high performance sensing, and the present invention eliminates need for a separate integrated circuit chip alongside the micromechanical device chip for complete system operation. The process of the basic invention can be implemented with on-chip integrated circuits as shown in Figures 5A-5H and Figures 6A-6I. The process in Figures 5A-5H allows a wafer first to be processed to include a fully functional integrated circuit and circuit components; thereafter, a micromechanical device is formed on the wafer using the basic invention. A basic restriction on this integration process is that the temperatures achieved in processing the micromechanical device must not damage the existing circuits. Usually, this requires that process temperatures not exceed 360°C, or approximately the temperature at which silicon and aluminum react. At even higher temperatures, such as 600°C, the aluminum metal leads typically used in integrated circuits will melt, rendering the circuit useless. Accordingly, the process temperatures achieved in the micromechanical device process must not exceed

350°C.

In Figure 5A, it is assumed that a conventional integrated circuit process has been completed on a silicon wafer 502, resulting in a functional circuit. A passivation dielectric layer 504, preferably silicon dioxide, remains on the wafer after the process to protect the circuit. The edge of the integrated circuit in Figure 5A is represented by the metal pad 506, connected, for example, to circuit layer 508. The wafer 502 includes a region 510 which is left free from circuit components and this is where the micromechanical structure is to be placed. A contact region 512 for metal to silicon contacts in the micromechanical structure is prepared prior to micromechanical device fabrication during the integrated circuit process to eliminate the high temperature implant anneal step which would damage a previously existing integrated circuit. The basic process of the invention now proceeds as in Figure 1, starting with the lithographic definition of an isolation trench 514 in a resist layer 516. The pattern is transferred to the dielectric layer 504 by reactive ion etching.

In Figure 5B, an isolation trench 518 is formed by the deep silicon etch techniques described earlier. The trench 518 may be tapered to match with the trench filling process depicted in Figure 5C. Because of the high temperature restrictions, the dielectric 520 filling the trench 518 must be deposited using low temperature chemical vapor deposition techniques. Techniques such as plasma enhanced chemical vapor deposition (PECVD) of TEOS and high density plasma chemical vapor deposition (HDPCVD) can fill high aspect ratio trenches at temperatures less than 300°C. The deposition process will often leave a void 522, a thicker dielectric layer 524 on the surface of the wafer, and an indentation 526 on the surface 528 in the location of the isolation trench.

A planarization sequence, as illustrated in Figure 5D, removes part of the dielectric layer 524 to form a new layer 530 and leaves a flat surface 532, ensuring that lithography and metal deposition steps to follow are free of any topographic effects. In Figure 5E, a second lithographic step forms contact vias 534 and 536. A photoresist 538 is exposed and developed, and a via pattern is transferred through the dielectric 530. The via pattern exposes both contact region 512, where contact is to be made to the silicon beams, and metal pad 506, where the integrated circuit is accessed.

After the photoresist is stripped, a metal layer 540 is sputter deposited to form contacts 542 and 544, as illustrated in Figure 5F. It is understood that this is a sample beam cross section only, and not all beams comprising the micromechanical device will require connection to the integrated circuit at 544. By opening vias to both the integrated circuit pad 506 and the micromechanical silicon contact 512, and using the metal layer 540, the integrated circuit is electrically connected to the micromechanical structure. A low temperature sintering step is commonly used to activate the contacts.

Figure 5G illustrates the coarse metal patterning step used to define the conduction paths on the micromechanical structure. Resist 546 is exposed and developed, and the resulting pattern is transferred to the metal in region 548. This step separates the metal segment 550 from the metal segment 552, creating a multiplicity of metal paths comprising the interconnect geometry for the micromechanical structure. Finally, in Figure 5H the micromechanical beam 554 is etched according to the process described in Figure 2, the resist pattern 556 being transferred through the metal, dielectric, and silicon layers using reactive ion etching. The beams are then released with a sidewall passivation and isotropic etching sequence to produce a cavity 558 separating the beam 554 and the substrate 502.

The filled isolation trench 518 separates the silicon of the micromechanical structure from the substrate silicon 502 and from the functional devices of the integrated circuit.

The process as described in Figure 5 achieves complete separation of the integrated circuit and micromechanical device fabrication steps. Another process for integration is illustrated in Figures 6A-6I, where the isolation trench is etched and filled prior to formation of the integrated circuit. The process follows those of Figure 1 and Figure 5 but varies in that the basic isolation process is interrupted to form the integrated circuit. It is described as follows:

As illustrated in Figure 6A, a silicon wafer 602 has a dielectric mask layer 604 and resist layer 606 which are used to define an isolation trench opening 608 using photolithography. The silicon isolation trench 610 in Figure 6B is etched, using the aforementioned techniques, through the mask opening 608. Figure 6C depicts the trench fill as dielectric 612 is deposited in trench 610, preferably using high temperature thermal oxidation. Since at this point in the process no integrated circuits exist, high temperature steps can still be performed. The thermal oxidation leaves a surface dielectric layer 614, and an indentation 616 in the region of the trench. The indentation and top surface dielectric is completely removed using planarization, resulting in a silicon wafer 602 with a polished silicon surface 618 and integral filled isolation trench 620, illustrated in Figure 6D. The planarization can be performed with deposition and etchback as described earlier or with chemical-mechanical polishing.

At this juncture the integrated circuit and circuit components are fabricated in accordance with known practice. As illustrated in Figure 6E, the location of the isolation segment 620 is spaced away from that of the integrated circuit, and its

presence has no effect on the circuit fabrication processes. The integrated circuit incorporates a metal pad 622 shown connected to a sample junction 624. Also created during the circuit fabrication is a dielectric passivation layer 626 and a contact region 628. The passivation layer 626 may be used as the micromechanical device insulator or replaced with a similarly deposited dielectric. The process then proceeds as described in Figures 5E-5H. In Figure 6F, vias 630 and 632 are created in the resist 634 and are transferred through the dielectric 626 to expose the integrated circuit metal pad 622 and contact region 628. After the resist is stripped, a metal layer 636, preferably aluminum, is sputter deposited in Figure 6G, contacting the integrated circuit metal pad 622 at the surface 638 and the silicon beam contact region 628 at the surface 640. In Figure 6H, the metal is coarsely patterned in the region 642 using the photoresist layer 644 and wet chemical or reactive ion etching. The micromechanical beam structure 646 is formed in Figure 6I using the resist patterned structure layer 648 and the series of etch and passivation steps described in Figures 1, 2, and 5. The resulting beam structures are free standing over the substrate 602 and are electrically isolated from the silicon substrate and the integrated circuit by the filled isolation trench 620.

Although the invention has been described in terms of preferred embodiments, it will be apparent to those of skill in the art that numerous variations and modifications may be made without departing from the true spirit and scope thereof, as set forth in the following claims.

What is claimed is:

1. A process for fabricating microstructures incorporating electrical isolation segments, comprising:

forming an isolation trench in a wafer;

filling the isolation trench with a dielectric material; and

forming in said wafer at least one released micromechanical beam which incorporates said isolation trench, whereby said dielectric material extends completely through said beam.

2. The process of claim 1, wherein forming an isolation trench includes:

defining an isolation trench pattern on an oxide coated silicon wafer;

transferring the pattern to the oxide; and

etching the wafer through the pattern in the oxide to form the isolation trench.

3. The process of claim 2, further including controlling said etching of the wafer to produce an isolation trench having a reentrant profile.

4. The process of claim 3, wherein filling the isolation trench includes thermally oxidizing the wafer.

5. The process of claim 3, wherein filling the isolation trench includes depositing a dielectric material by chemical vapor deposition.

6. The process of claim 1, wherein filling the isolation trench includes thermally oxidizing the wafer.

7. The process of claim 1, further including planarizing the wafer after filling said isolation trench.

8. The process of claim 7, wherein planarization includes application of a viscous material to said wafer and etching back said viscous material to smooth small nonuniformities.

9. The process of claim 1, further including providing a layer of dielectric on said wafer to serve as a mask for forming said isolation trench.

10. The process of claim 9, wherein forming at least one micromechanical beam includes coating said layer of dielectric on said wafer with a layer of material;

patterning and etching said metal and said dielectric layers to define a beam to be released;

etching said wafer through said patterned metal layer to produce a mesa corresponding to said micromechanical beam; and

further etching said mesa to undercut it and to produce a released micromechanical beam.

11. The process of claim 10, further including producing at least one via in said \ dielectric at said beam to be released prior to coating with said layer of metal to permit said metal to contact said released beam.

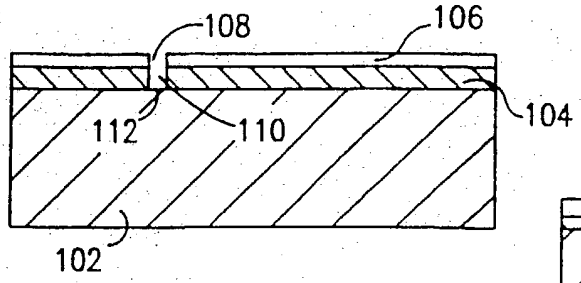


FIG. 1A

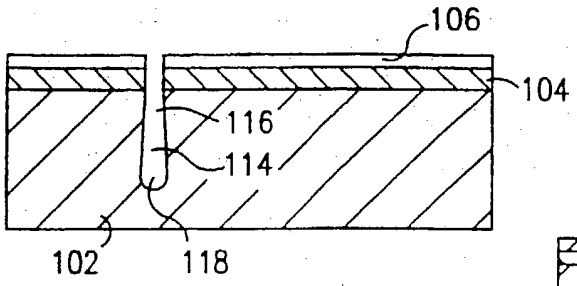


FIG. 1B

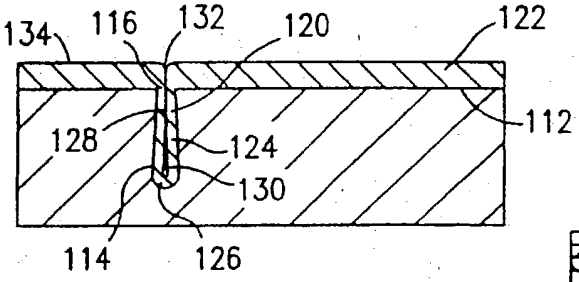


FIG. 1C

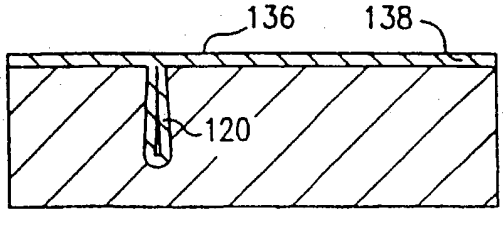


FIG. 1D

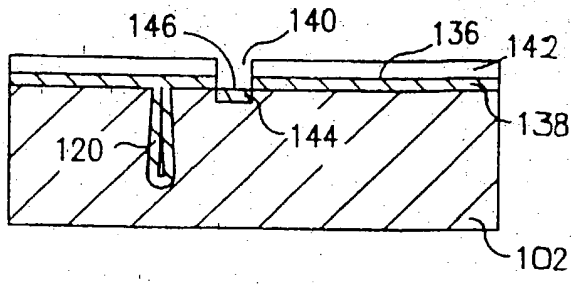


FIG. 1E

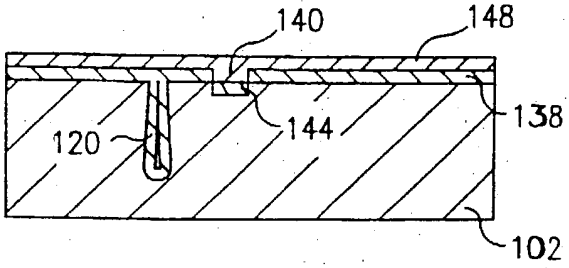


FIG. 1F

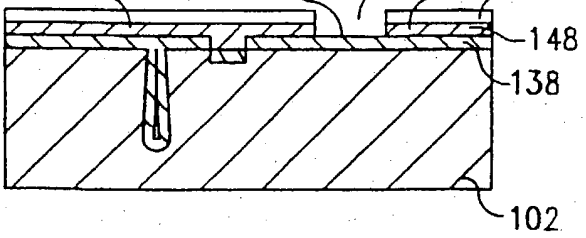


FIG. 1G

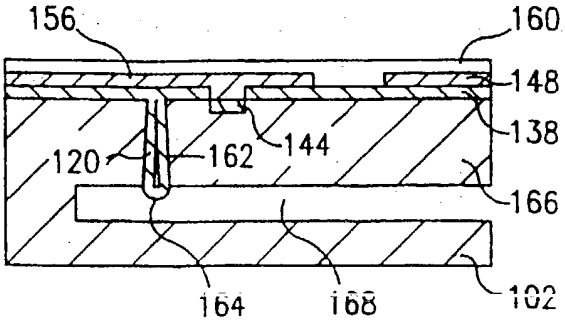


FIG. 1H

FIG. 2A

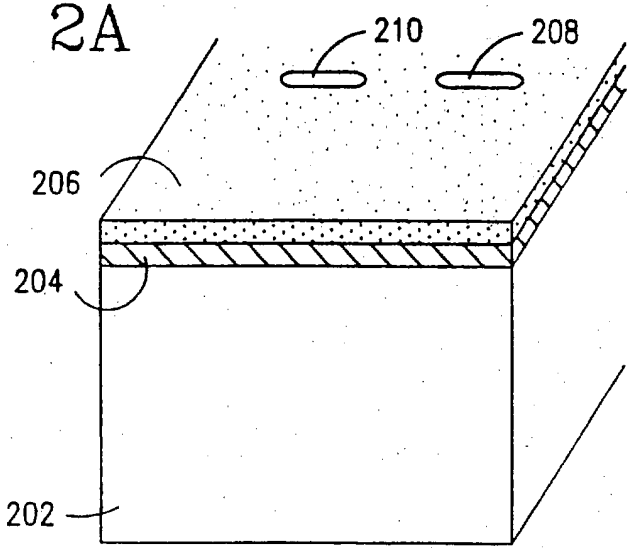


FIG. 2B

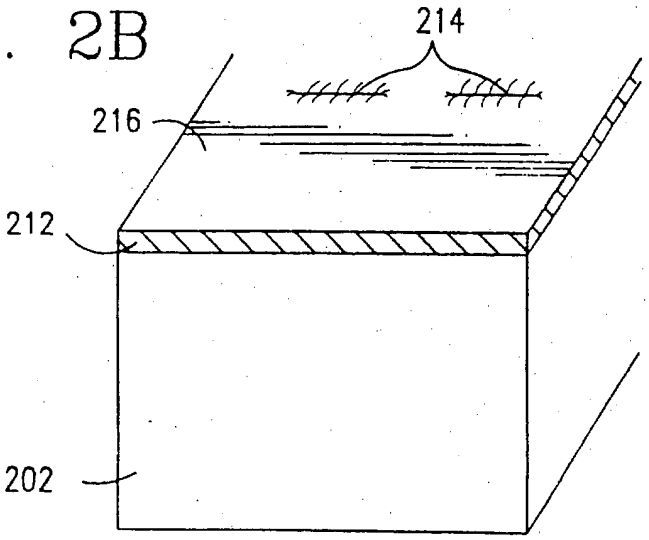


FIG. 2C

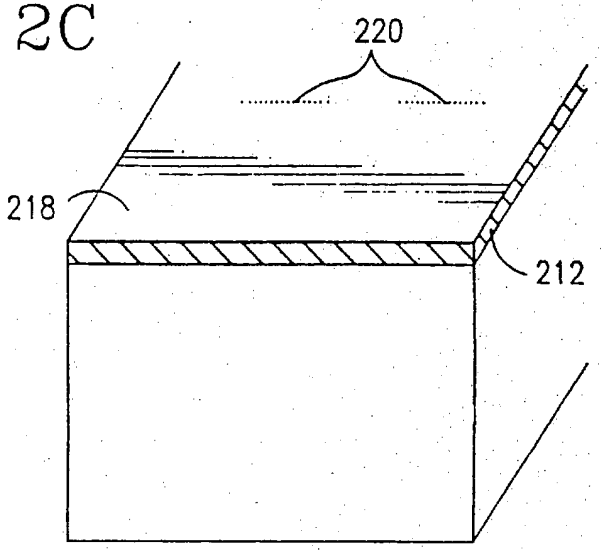


FIG. 2D

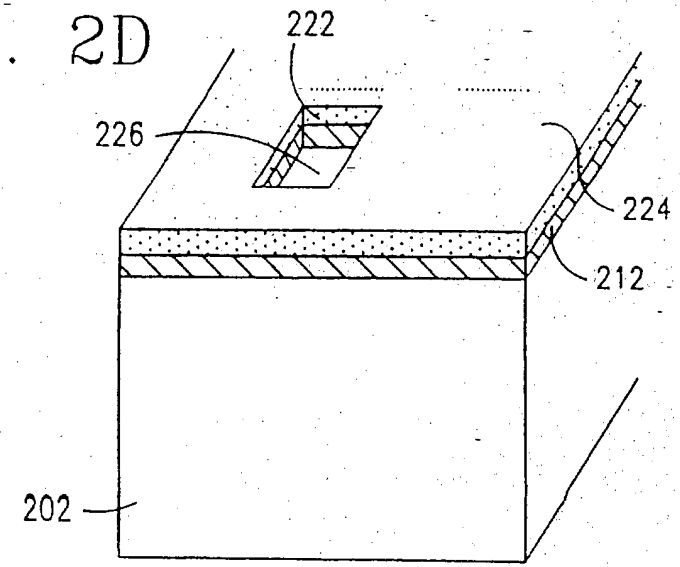


FIG. 2E

FIG. 2F

FIG. 2G

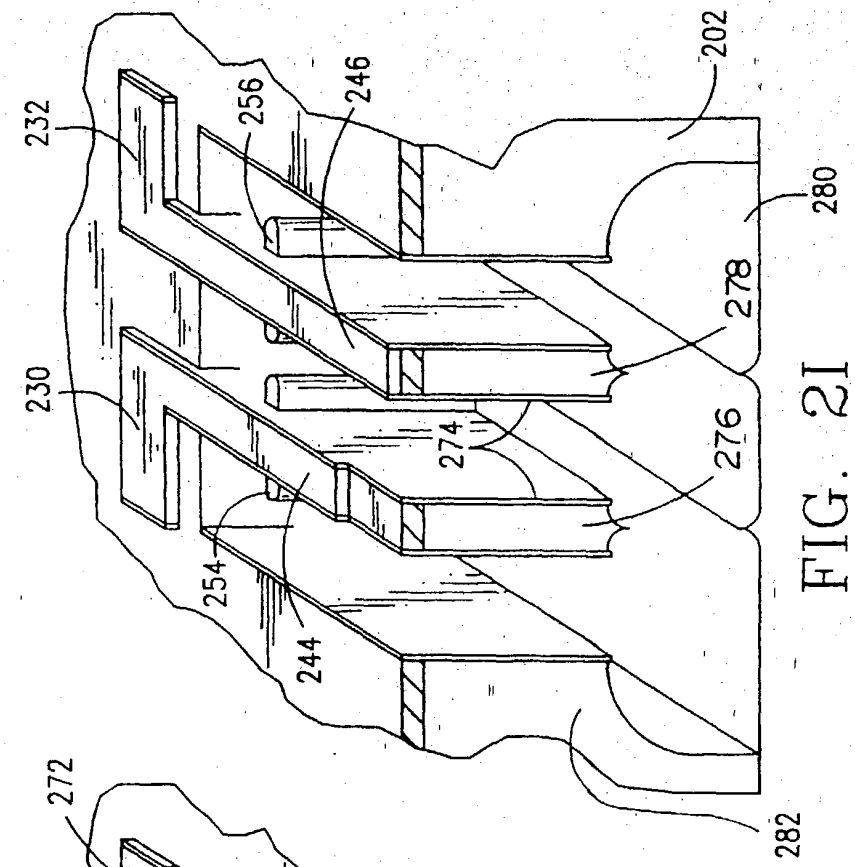

232
256
246
202
280
278
230
274
276
254
244
282

FIG. 2I

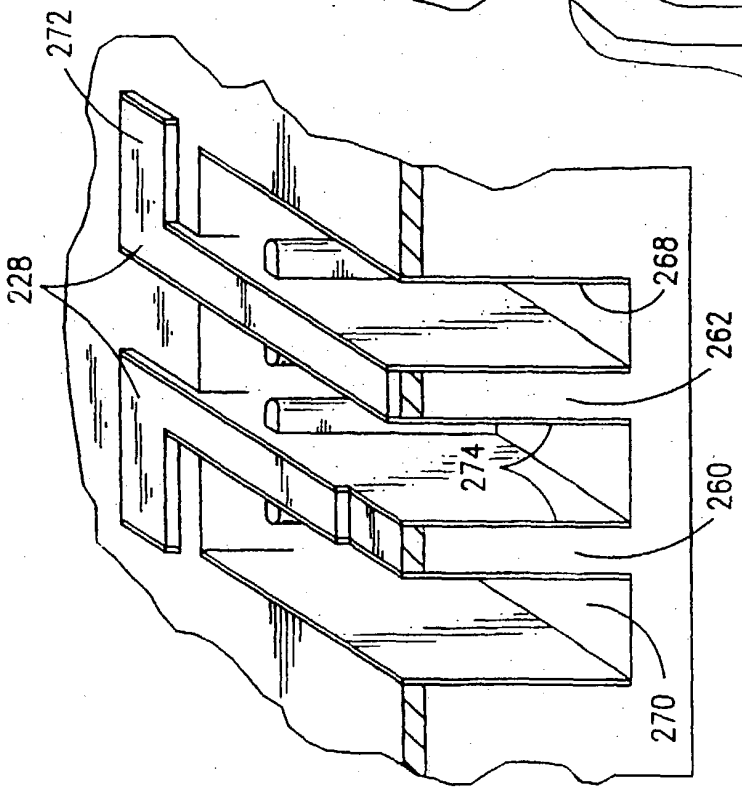

272
228
268
262
274
260
270

FIG. 2H

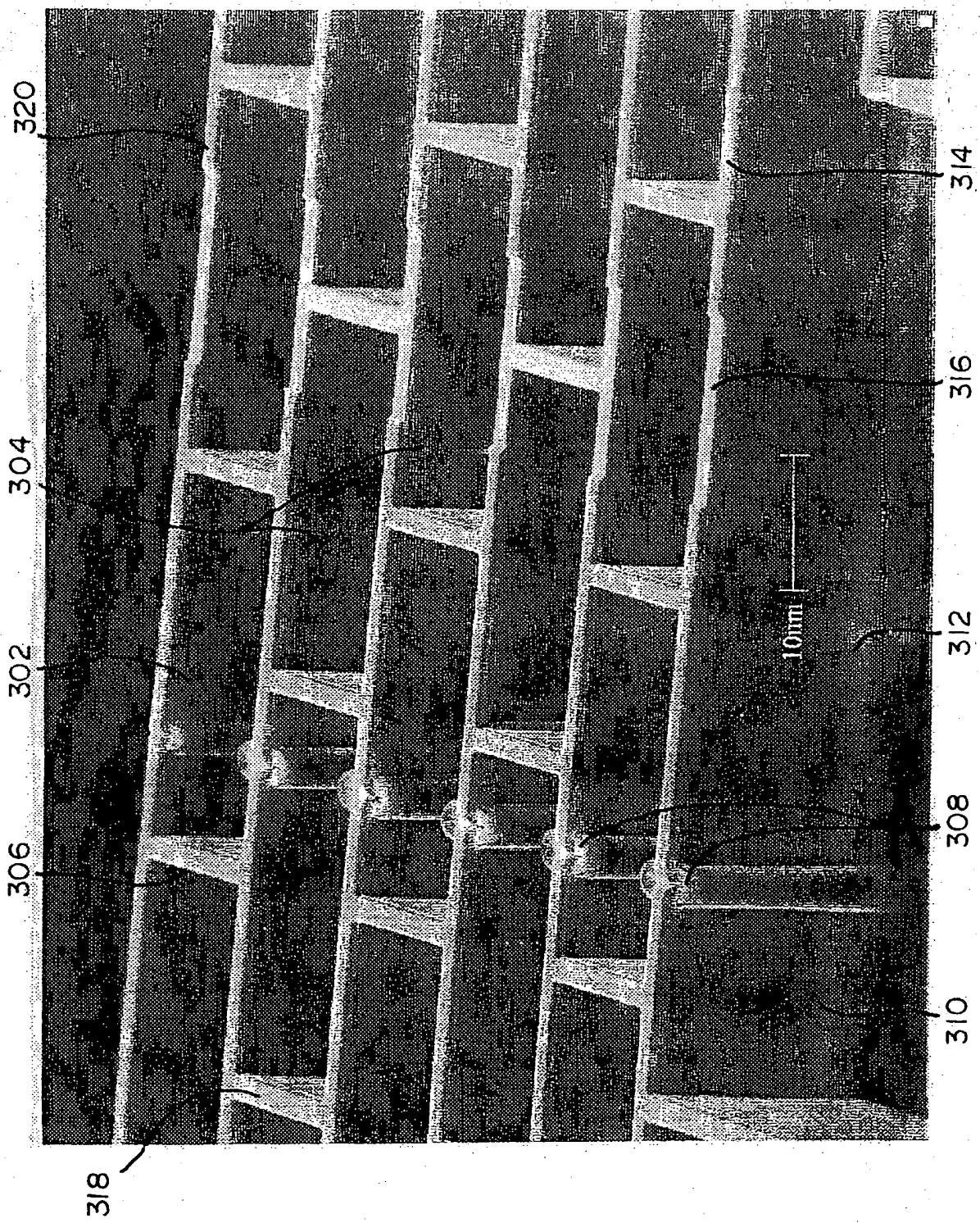


FIG. 3

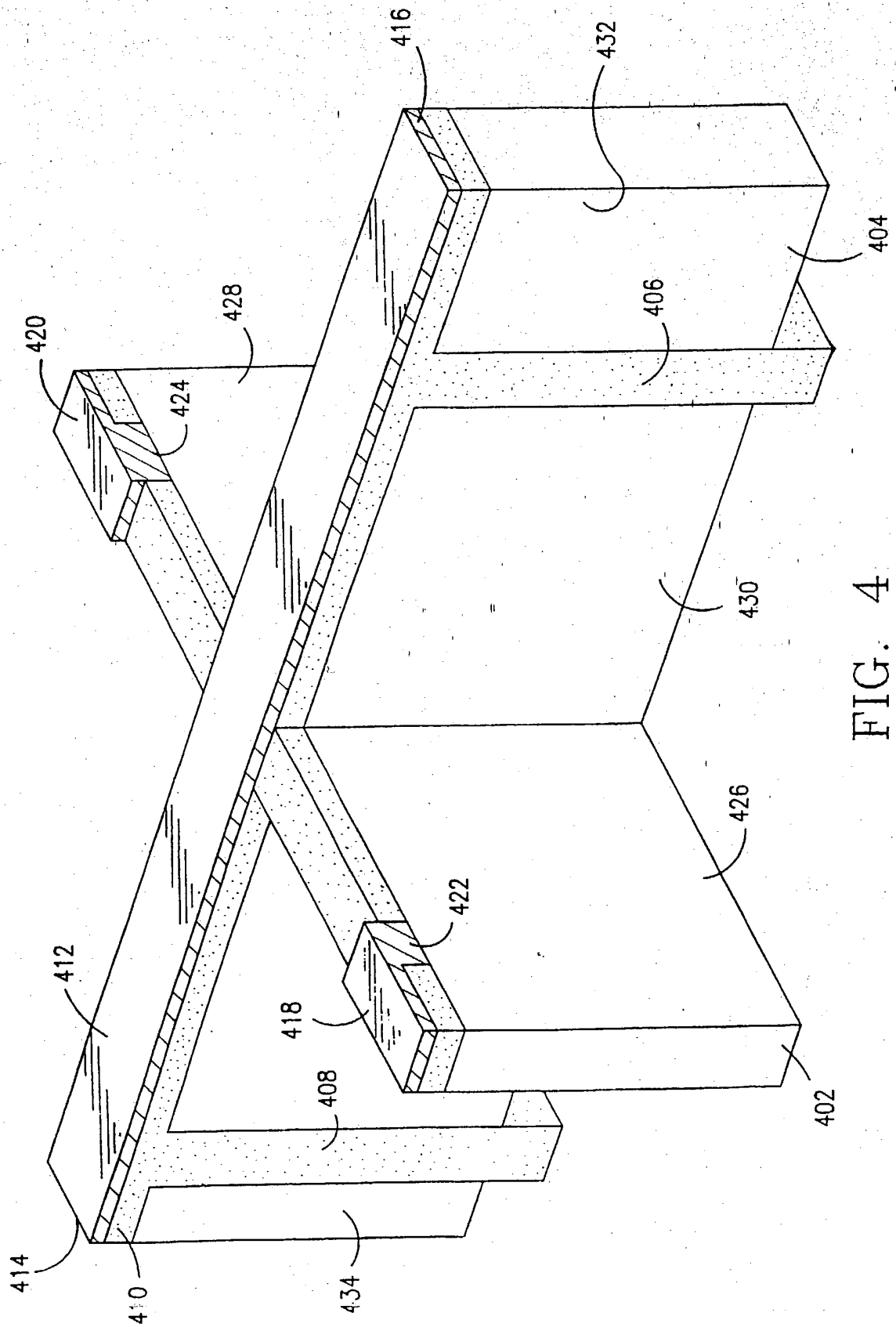

416
432
404
406
428
420
424
430
426
422
412
418
408
402
414
410
434

FIG. 4

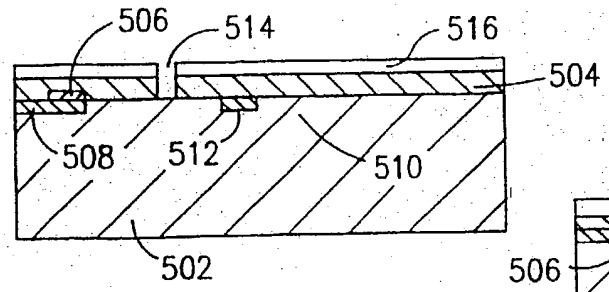


FIG. 5A

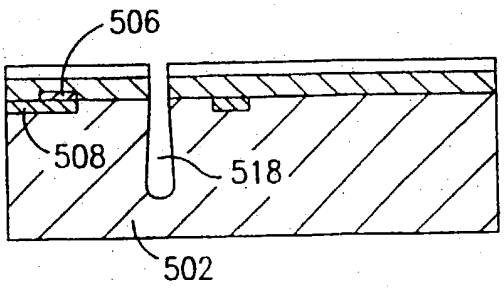


FIG. 5B

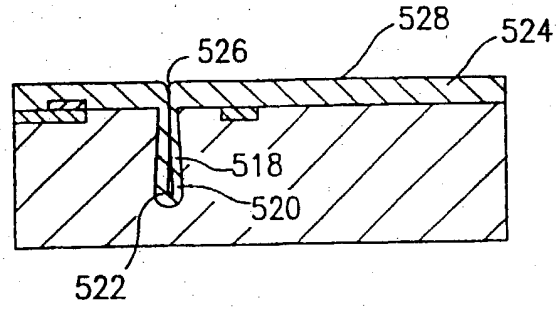


FIG. 5C

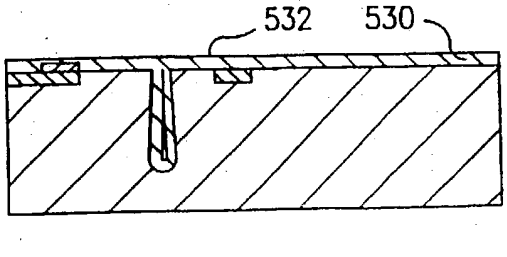


FIG. 5D

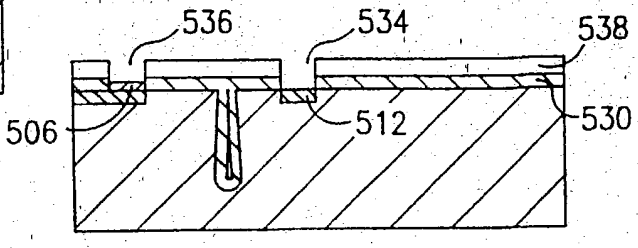


FIG. 5E

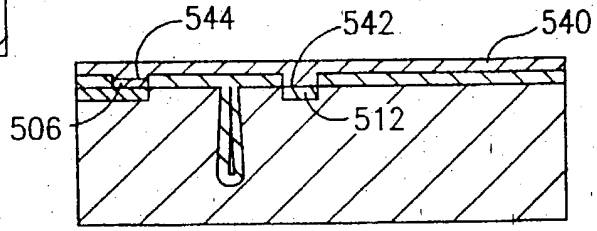


FIG. 5F

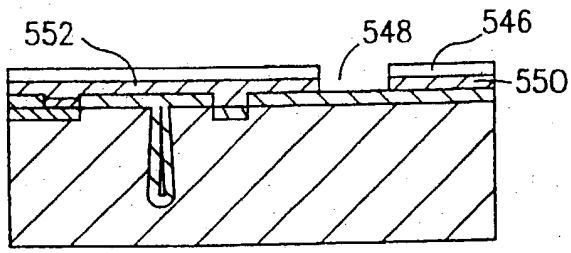


FIG. 5G

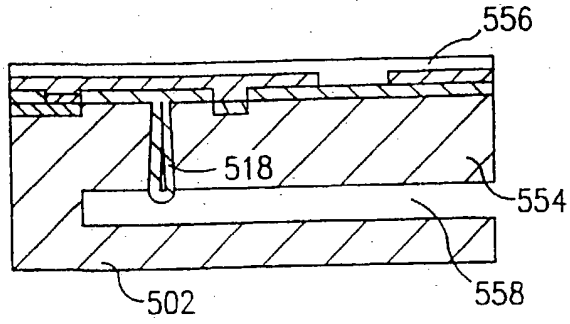


FIG. 5H

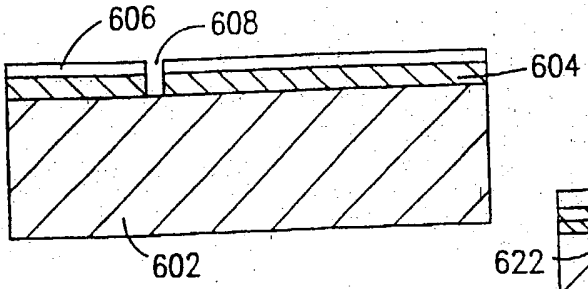


FIG. 6A

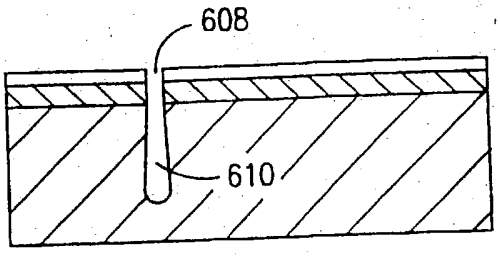


FIG. 6B

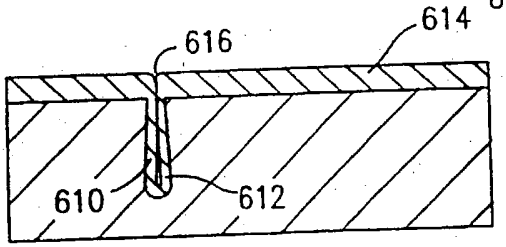


FIG. 6C

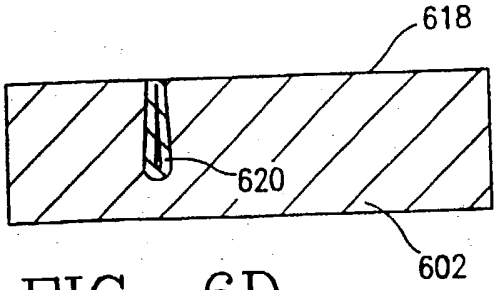


FIG. 6D

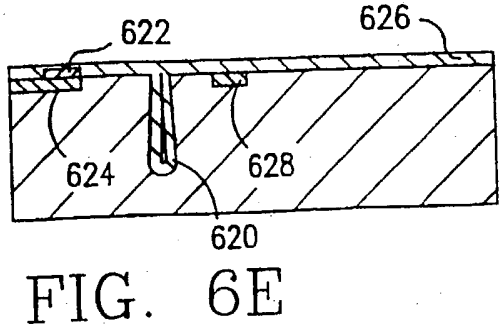


FIG. 6E

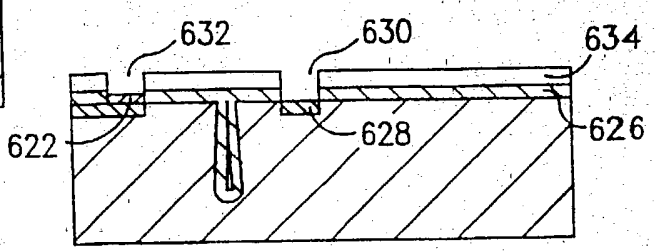


FIG. 6F

FIG. 6G

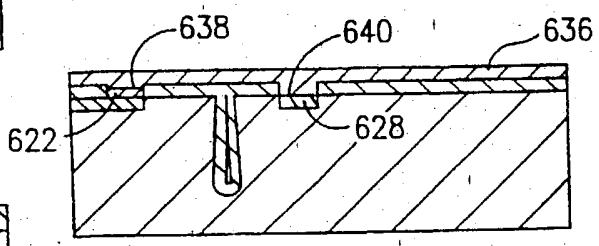


FIG. 6H

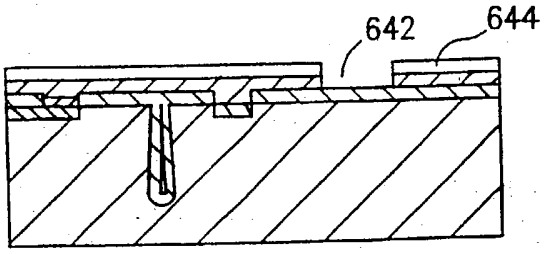


FIG. 6I